code word is complete, the error corrector 6 transmits the one-code word error correction completion signal 23 to the DMA control unit 2 and to the error detector 7.

Step (d-9): in response to the output of the one-code word error correction completion signal 23, the DMA control unit 2 outputs the DMA request 13 to the bus control unit 3 so as to request the transfer of the error-corrected code word from the buffer memory 4 to the error corrector 7.

Step (d-10): after putting the data bus 11 in commission, the bus control unit 3 outputs the buffer memory access signal 14 to the buffer memory 4 to read the data therefrom. Then, the bus control unit 3 outputs the error detector data supply signal 20 to the error detector 7 so as to supply the data read from the buffer memory 4.

Step (d-11): while using the mid-term results of error correction stored in the mid-term result register 8, the error detector 7 executes error detection for the transferred subsequent data up to and including the final code word.

Step (d-12): upon completion of the DMA transfer to the error detector 7, the DMA control unit 2 resumes the output of the DMA request 13 transferring the subsequent code words to the syndrome calculator 5 and to the error detector 7. The bus control unit 3 executes a data transfer from the buffer memory 4 to the syndrome calculator 5 and to the error detector 7.

The operations at steps (d-4) through (d-12) are repeated until error correction for one sector is complete.

When the error correction for one sector is complete, the error

corrector 6 outputs the error correction completion signal 19 to the system control unit 1, and the error detector 7 informs the system control unit 1 whether an error has been detected or not by transmitting the error detection signal 21.

When an error-containing code has not been detected in the syndrome calculator 5 at step (d-4), the error correcting operations between steps (d-5) and (d-8) are executed concurrently with the operation at step (d-4); however, the error correcting operation for data on the buffer memory 4 and the DMA transfer are not suspended because an error-containing code has not been detected. The error detection of the error detector 7 is complete at step (d-4), and it is informed to the system control unit 1 by transmitting the error detection signal 21 that no error has been detected. In this case, steps (d-9) through (d-12) are not executed.

Through these steps, horizontal error correction for one sector is complete. In the same manner, horizontal error correction is executed for the subsequent 15 sectors so as to complete the horizontal error correction for one block. If no error is detected from all sectors, the error correcting operation is complete; if there is an error detected even from one sector, the next process including vertical error correction will be executed.

As described hereinbefore, in the present embodiment, data are transferred from the buffer memory 4 not only to the syndrome calculator 5 but also to the error detector 7 at the same time, and until the syndrome calculator 5 detects an error-containing code, the error detector 7 executes error detection concurrently with syndrome calculation. If an error-containing code is detected by the syndrome calculator 5, the

syndrome calculation is suspended, and the error-containing code is corrected by the error corrector 6. Then, the data are transferred to the error detector 7 so as to be subjected to error detection. After the error detection, the subsequent code words are transferred to the syndrome calculator 5 and to the error detector 7 where syndrome calculation and error detection are executed in parallel.

Thus, when an error-containing code word has been detected, the error-corrected data of the code word can be exclusively re-transferred to the error detector 7 so as to execute a series of processes including error-containing code detection, error correction, and error detection in parallel, thereby greatly reducing the time required for error correction.

(Embodiment 4)

The present embodiment provides two buffer memories in order to reduce the time required for reading and writing data; while data are being read from or written to one of the buffer memories, data in the other buffer memory are subjected to error correction.

The structure of the main part of the error correction device of the present invention is shown in Figure 11. The error correction device comprises a downstream processing unit 9 composed of a transfer control device and the like, an upstream processing unit 10 composed of a demodulator and the like, a first buffer memory 41 provided with an overwrite unit and a readout unit, and a second buffer memory 42 provided with an overwrite unit and a readout unit. The device further comprises a buffer switch control unit 101, a buffer data transfer control unit 102, and an initial setting unit 103 which are arranged in the system control unit 1.